Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(withdrawn) A process for manufacturing a twin gain bipolar transistor, comprising:

providing a P type silicon wafer having an upper surface;

implanting first donor ions through said upper surface;

performing a first drive-in diffusion thereby forming an N+ buried collector that is between about 3 and 4 microns thick and having an upper N-to-N+ interface that is between about 0.8 and 1 microns below said wafer upper surface;

depositing a layer of boron doped silicon by means of epitaxial growth on said wafer upper surface, thereby forming a P type secondary base layer that contains a uniform distribution of acceptors and has an upper surface;

forming a first oxide layer on said it epitaxial layer upper surface;

patterning the first oxide layer by photolithography to form a first mask;

through said first mask, implanting boron ions;

performing a second drive-in diffusion whereby a primary base layer is formed within the secondary base layer;

removing the first mask;

forming a second mask by photolithography on said epitaxial layer upper surface;

patterning to form an emitter mask;

through said emitter mask, implanting second donor ions; and

performing a third drive-in diffusion whereby an N+ emitter is formed within the

primary base layer.

2.(withdrawn) The process of claim 1 wherein the first donor ions are implanted at an energy between about 60 and 100 keV.

3.(withdrawn) The process of claim 1 wherein the implanted dosage of the first donor ions is between about 1×10^{15} and 5×10^{15} ions/cm^2.

4.(withdrawn) The process of claim 1 wherein said first drive-in diffusion further comprises heating at a temperature between about 1,100 and 1,200 °C for between about 180 and 300 minutes.

5.(withdrawn) The process of claim 1 wherein the epitaxial layer has a thickness between about 4 and 5 microns.

6.(withdrawn) The process of claim 1 wherein said epitaxial layer has an acceptor concentration between about 4×10^{15} and 5×10^{15} ions/cm^3, corresponding to a resistivity between about 30 and 60 ohm cm.

7.(withdrawn) The process of claim 1 wherein the implanted boron ions have an energy between about 30 and 40 keV and a implanted dosage between about 5×10^{12} and 1×10^{13} ions/cm^2.

8.(withdrawn) The process of claim 1 wherein the second drive-in diffusion comprises heating at a temperature between about 1,000 and 1,100 °C for between about 60 and 120 minutes.

9.(withdrawn) The process of claim 1 wherein said primary base layer extends to a depth between about 0.6 and 0.8 microns below the surface of the epitaxial layer.

10.(withdrawn) The process off claim 1 wherein the second implanted donor ions have an energy between about 60 and 65 keV and an implanted dosage between about 4 x 10^{15} and 7 x 10^{15} ions/cm^2.

11.(withdrawn) The process of claim 1 wherein the third drive-in diffusion comprises heating at a temperature between about 950 and 1,000 °C for between about 60 and 100 minutes.

12.(currently amended) A twin gain bipolar transistor comprising:

an N type silicon body having an upper surface;

an N+ buried collector located a first distance below said upper surface and having a thickness;

a secondary base region comprising P type silicon, throughout which boron ions are uniformly distributed, and extending a second distance below said upper surface;

a primary base region of boron doped P+ silicon, wholly within said secondary base region and extending a third distance below said upper surface, said third distance being less than said second distance; and

an emitter region comprising a region of N+ silicon wholly within the primary base region and extending a fourth distance below said upper surface.

13.(previously presented) The transistor described in claim 12 wherein said first distance is between about 630 and 732 microns.

14.(previously presented) The transistor described in claim 12 wherein the buried

collector has a thickness between about 4 and 5 microns.

15.(previously presented) The transistor described in claim 12 wherein the resistivity of the secondary base region is between about 30 and 60 ohm cm.

16.(previously presented) The transistor described in claim 12 wherein said second distance is between about 0.6 and 0.8 microns.

17.(previously presented) The transistor described in claim 12 wherein resistivity of the primary base region is between about 0.2 and 0.3 ohm cm.

18.(previously presented) The transistor described in claim 12 wherein said third distance is between about 0.6 and 0.8 microns.

19.(previously presented) The transistor described in claim 12 wherein said fourth distance is between about 0.3 and 0.35 microns.

20.(previously presented) The transistor described in claim 12 wherein said N type silicon body is an N type silicon wafer or an N well within a silicon wafer.